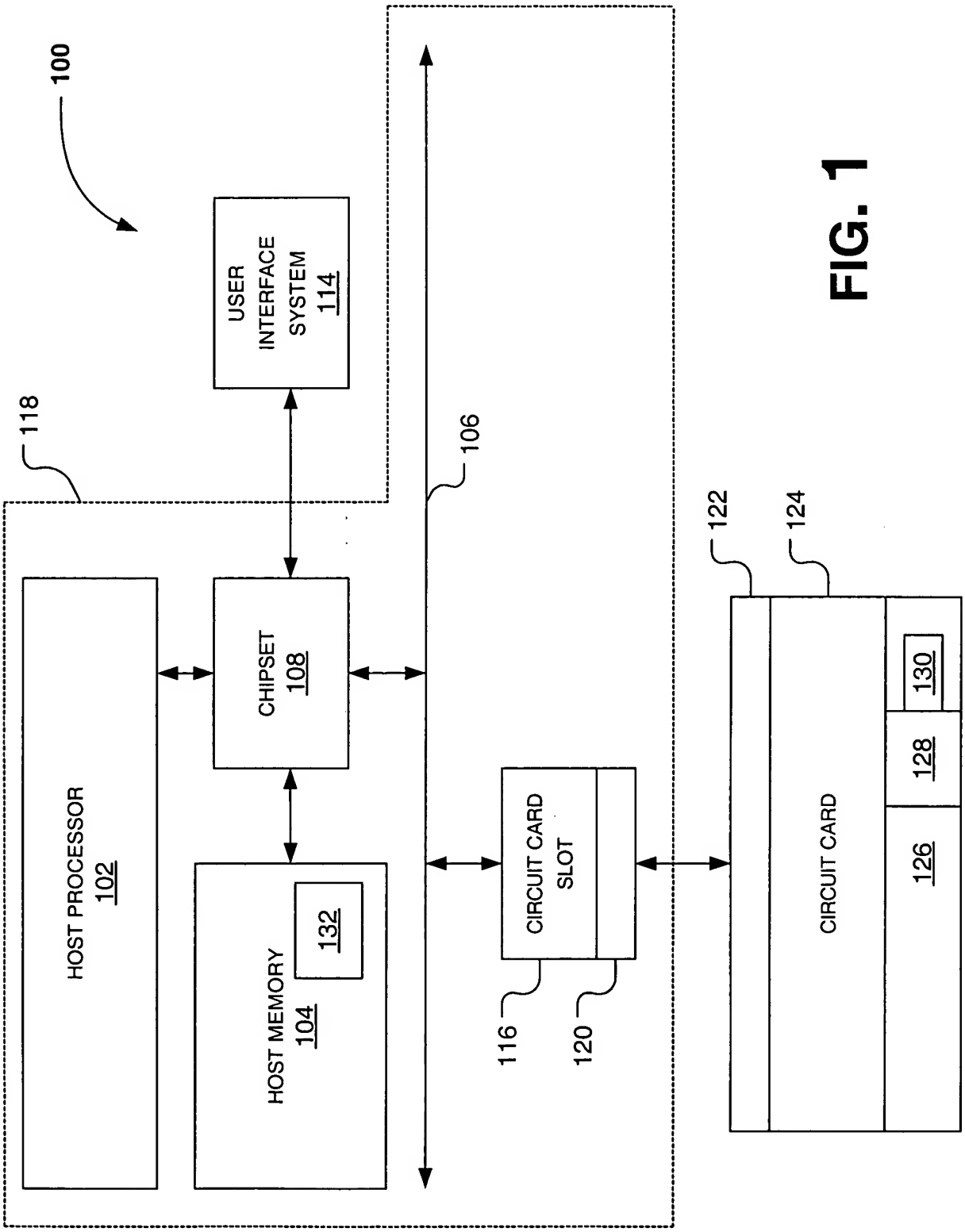
100
USER INTERFACE SYSTEM 114
118
106
122
124
CHIPSET 108
HOST PROCESSOR 102
HOST MEMORY 104
132
CIRCUIT CARD SLOT
CIRCUIT CARD
130
128
126
116
120

FIG. 1

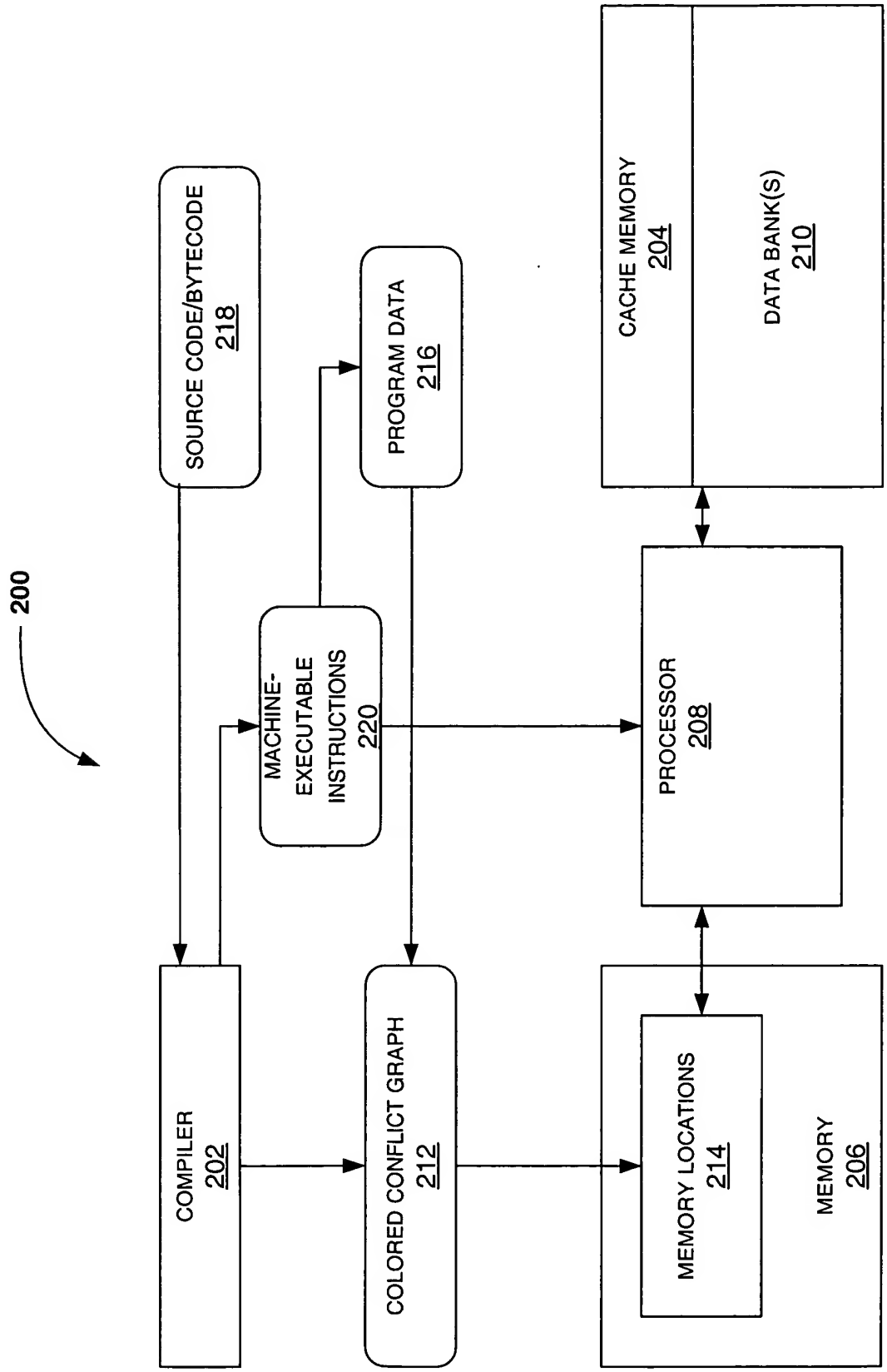
200
SOURCE CODE/BYTECODE 218
PROGRAM DATA 216
CACHE MEMORY 204
DATA BANK(S) 210
MACHINE-EXECUTABLE INSTRUCTIONS 220
PROCESSOR 208
COMPILER 202
COLORED CONFLICT GRAPH 212
MEMORY LOCATIONS 214
MEMORY 206

FIG. 2

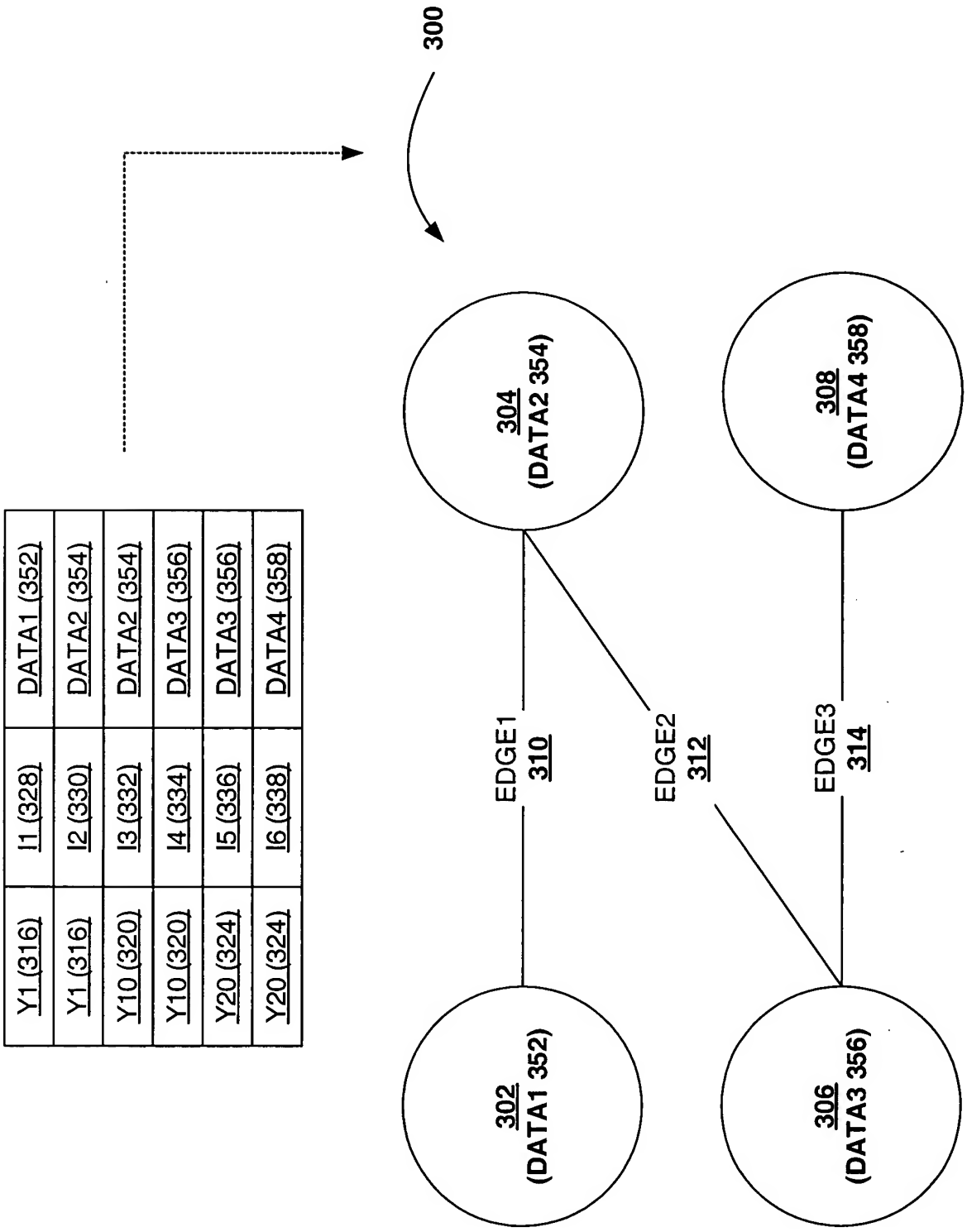
300
Y1 (316)
I1 (328)
DATA1 (352)
Y1 (316)
I2 (330)
DATA2 (354)
Y10 (320)
I3 (332)
DATA2 (354)
Y10 (320)
I4 (334)
DATA3 (356)
Y20 (324)
I5 (336)
DATA3 (356)
Y20 (324)
I6 (338)
DATA4 (358)
304 (DATA2 354)
308 (DATA4 358)
EDGE1 310
EDGE2 312
EDGE3 314
302 (DATA1 352)
306 (DATA3 356)

FIG. 3

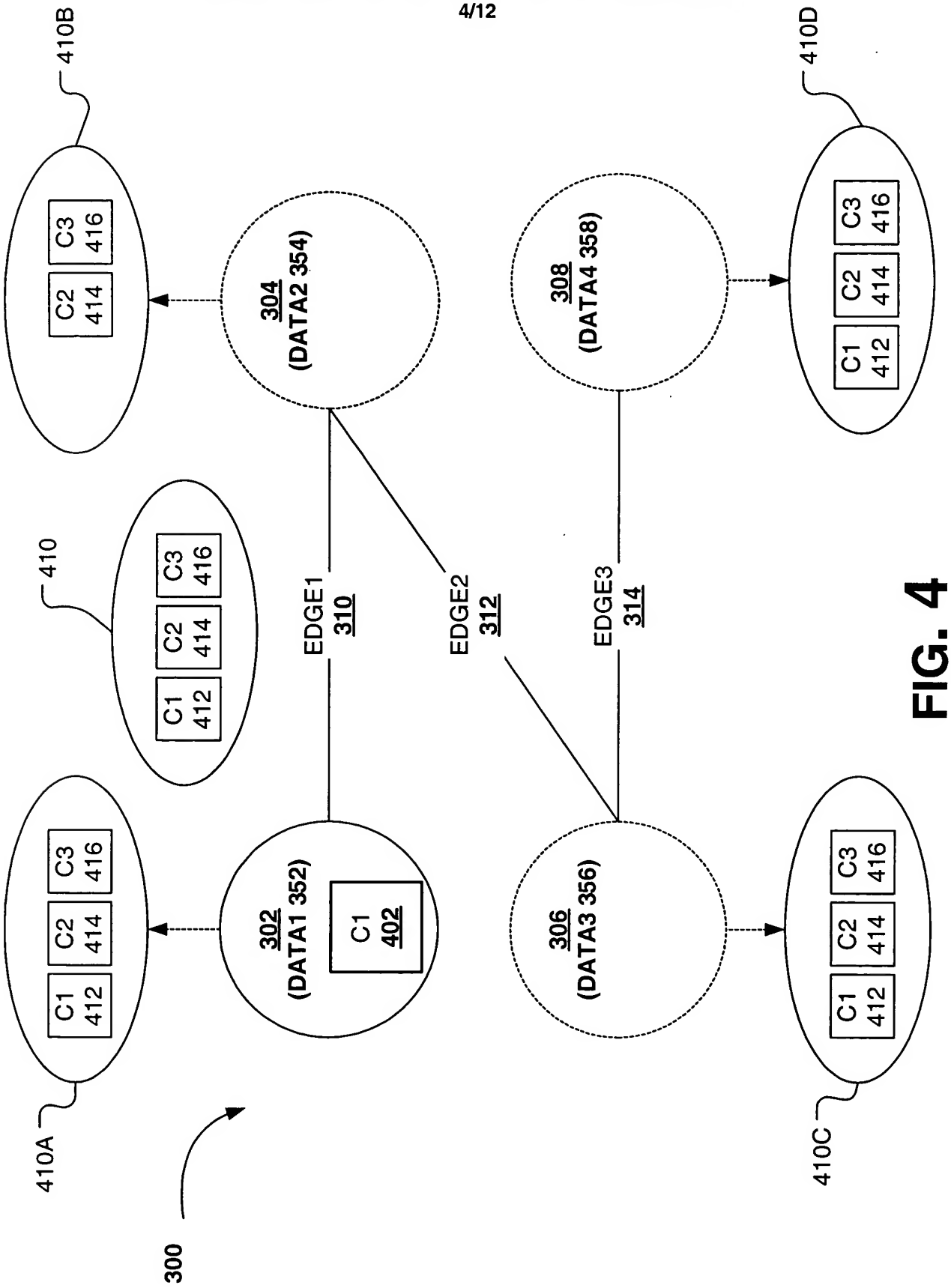
410B
C3 416
C2 414
304 (DATA2 354)
308 (DATA4 358)
410D
C1 412
410
EDGE1 310
EDGE2 312
EDGE3 314
302 (DATA1 352)
C1 402
306 (DATA3 356)
410A
410C
300

FIG. 4

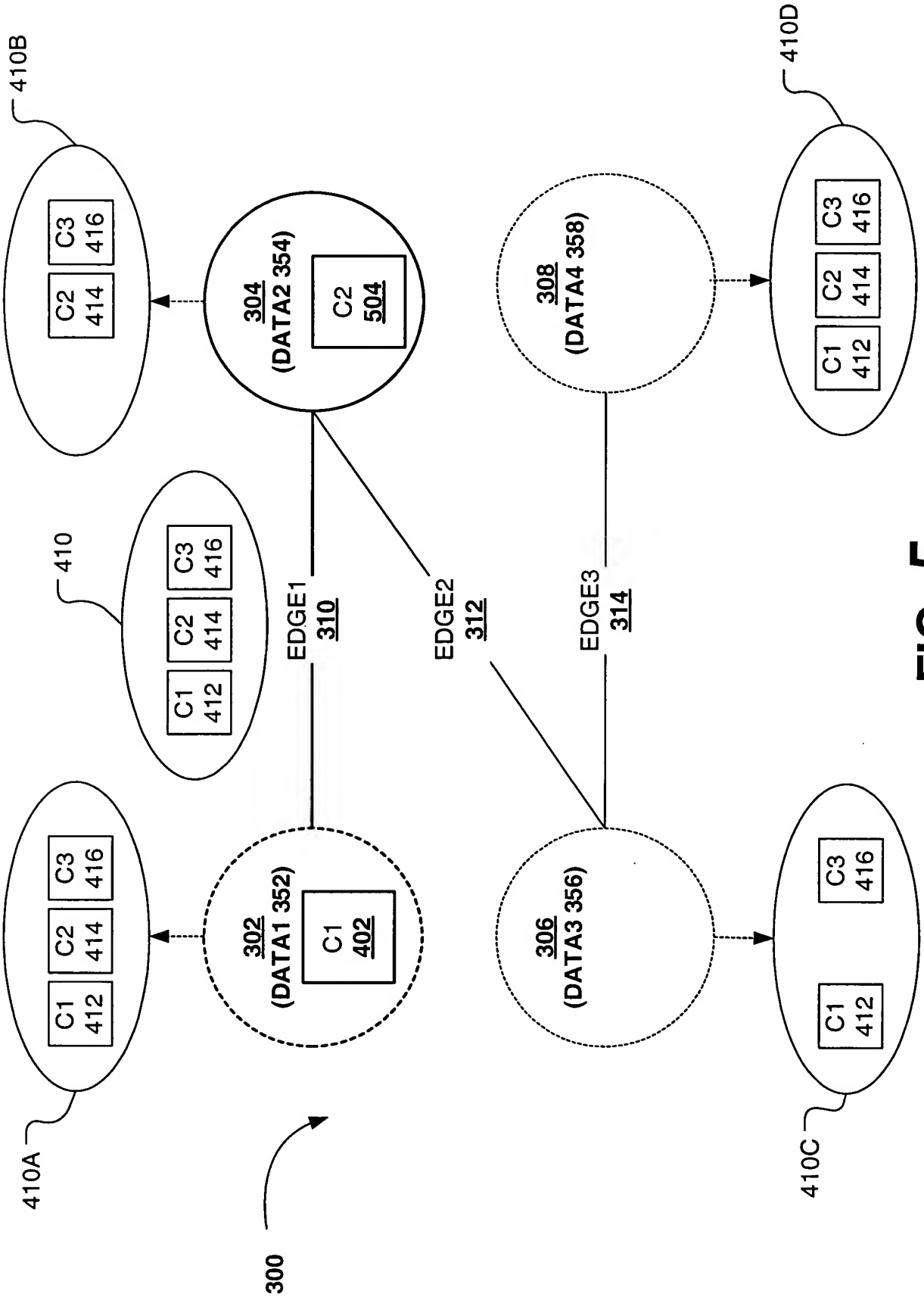
410B
C2 414
C3 416
304 (DATA2 354)
C2 504
410
C1 412
C2 414
C3 416
EDGE1 310
EDGE2 312
EDGE3 314
308 (DATA4 358)
410D
C1 412
C2 414
C3 416
302 (DATA1 352)
C1 402
306 (DATA3 356)
C3 416
C1 412
C1 412
C2 414
C3 416
410A
410C
300

FIG. 5

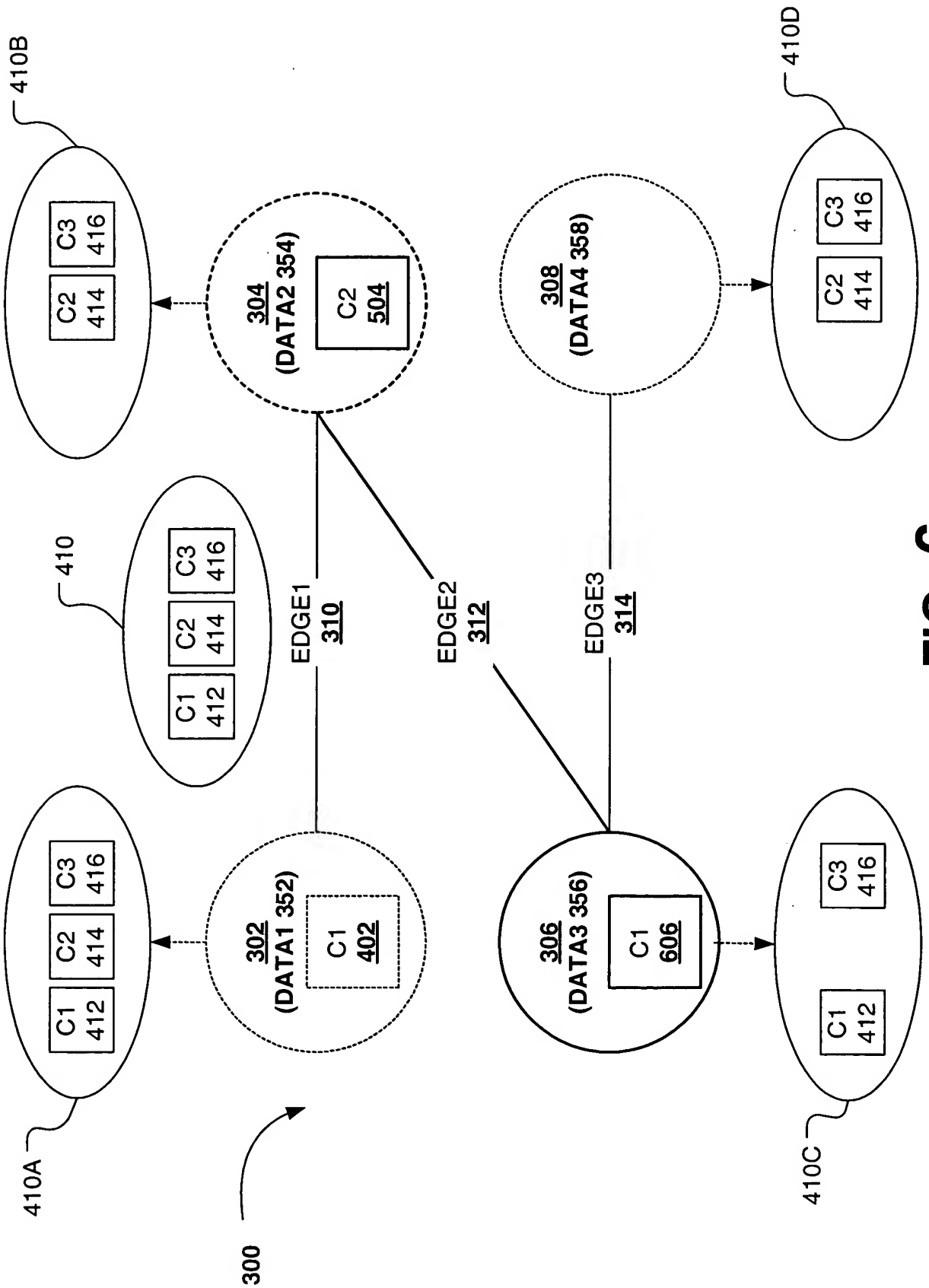
410B
C2 414
C3 416
304 (DATA2 354)
C2 504
308 (DATA4 358)
410D
C2 414
C3 416
410
C1 412
C2 414
C3 416
EDGE1 310
EDGE2 312
EDGE3 314
410A
C1 412
C2 414
C3 416
302 (DATA1 352)
C1 402
306 (DATA3 356)
C1 606
410C
C1 412
C3 416
300

FIG. 6

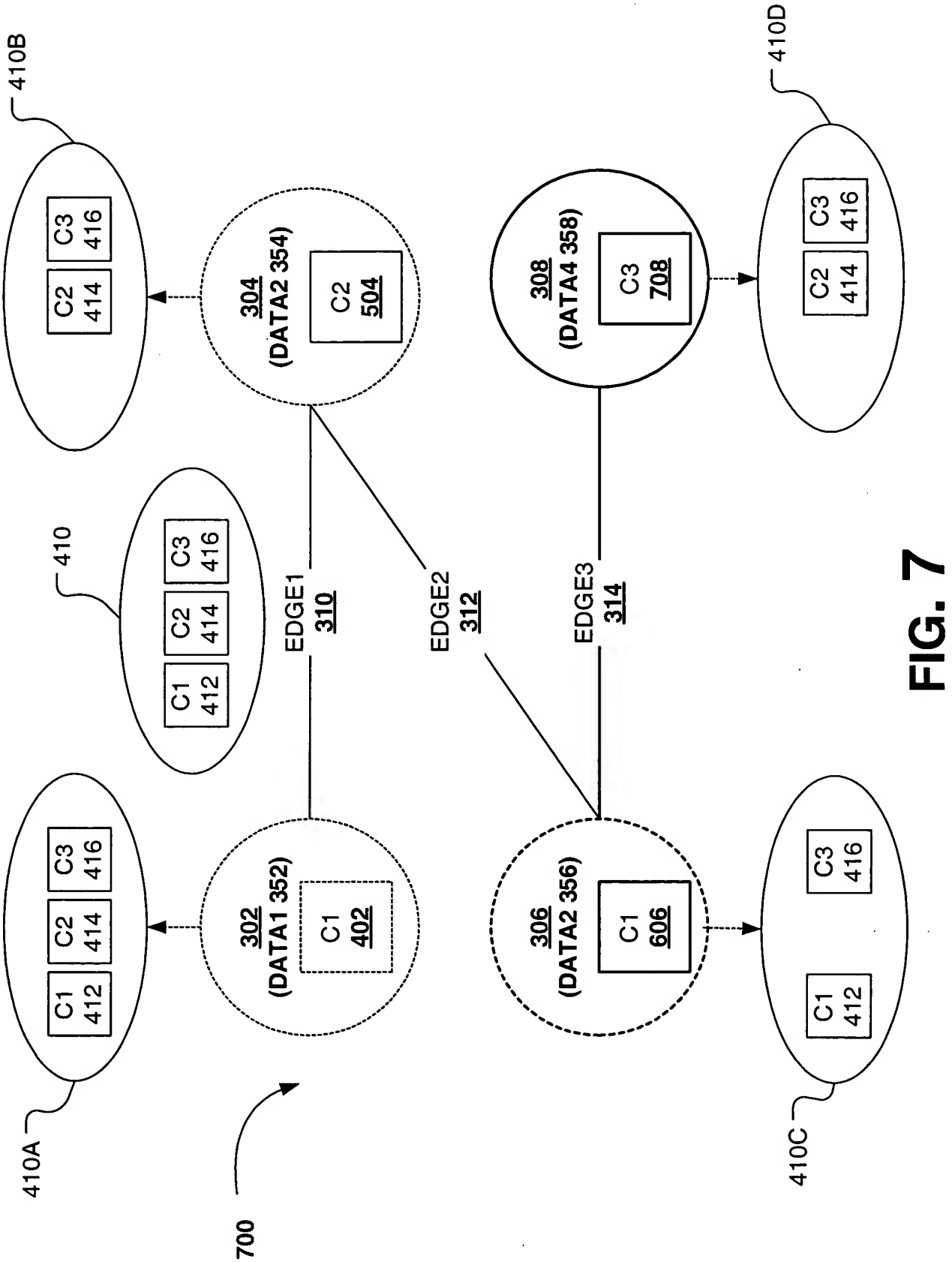
410B
C2 414
C3 416
304 (DATA2 354)
C2 504
410
C1 412
C2 414
C3 416
EDGE1 310
EDGE2 312
EDGE3 314
308 (DATA4 358)
C3 708
410D
C2 414
C3 416
302 (DATA1 352)
C1 402
306 (DATA2 356)
C1 606
C3 416
C1 412
C1 412
C2 414
C3 416
410A
410C
700

FIG. 7

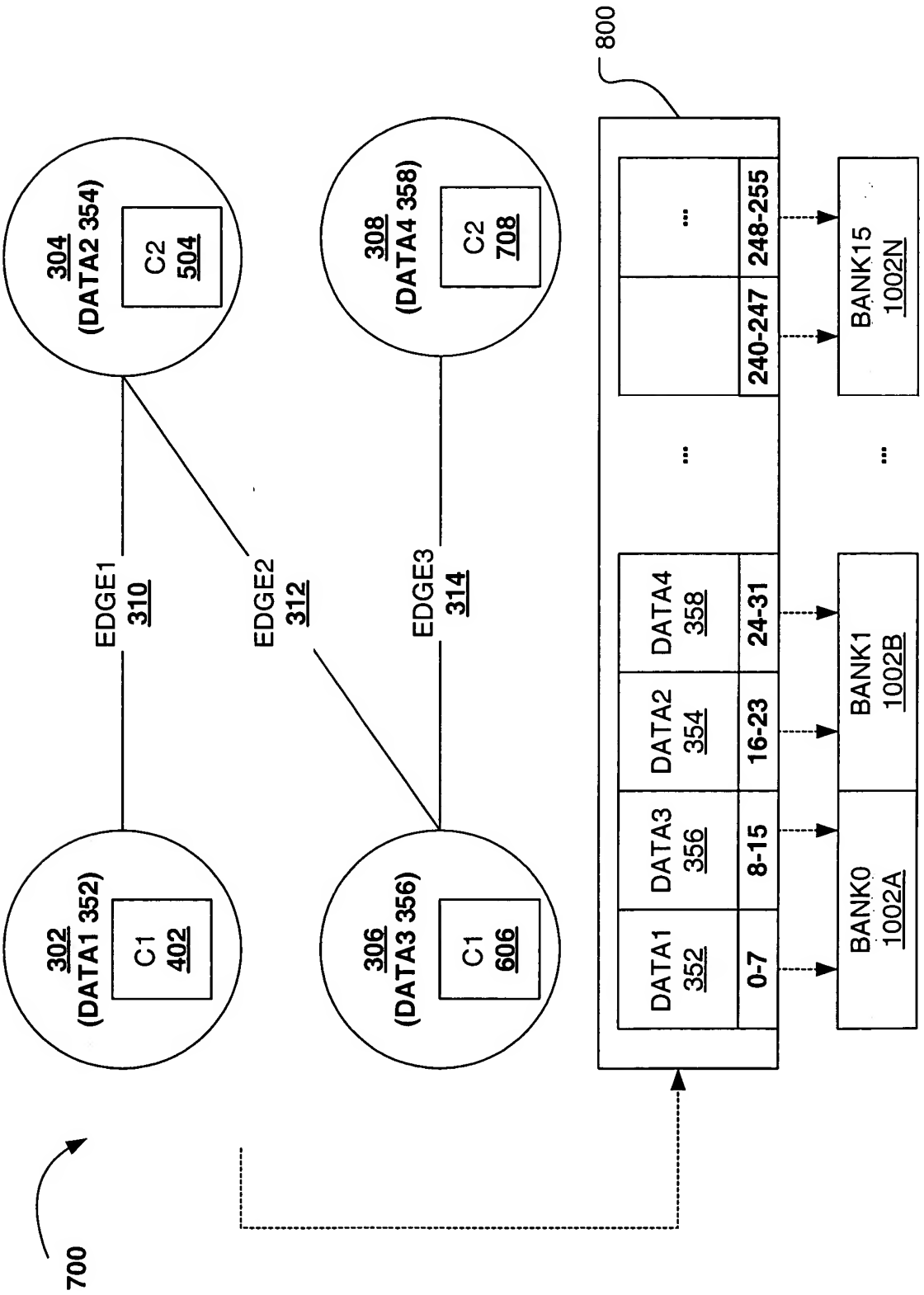
700
800
302 (DATA1 352)
C1 402
304 (DATA2 354)
C2 504
306 (DATA3 356)
C1 606
308 (DATA4 358)
C2 708
EDGE1 310
EDGE2 312
EDGE3 314
DATA1 352
DATA3 356
DATA2 354
DATA4 358
0-7
8-15
16-23
24-31
240-247
248-255
BANK0 1002A
BANK1 1002B
BANK15 1002N

FIG. 8

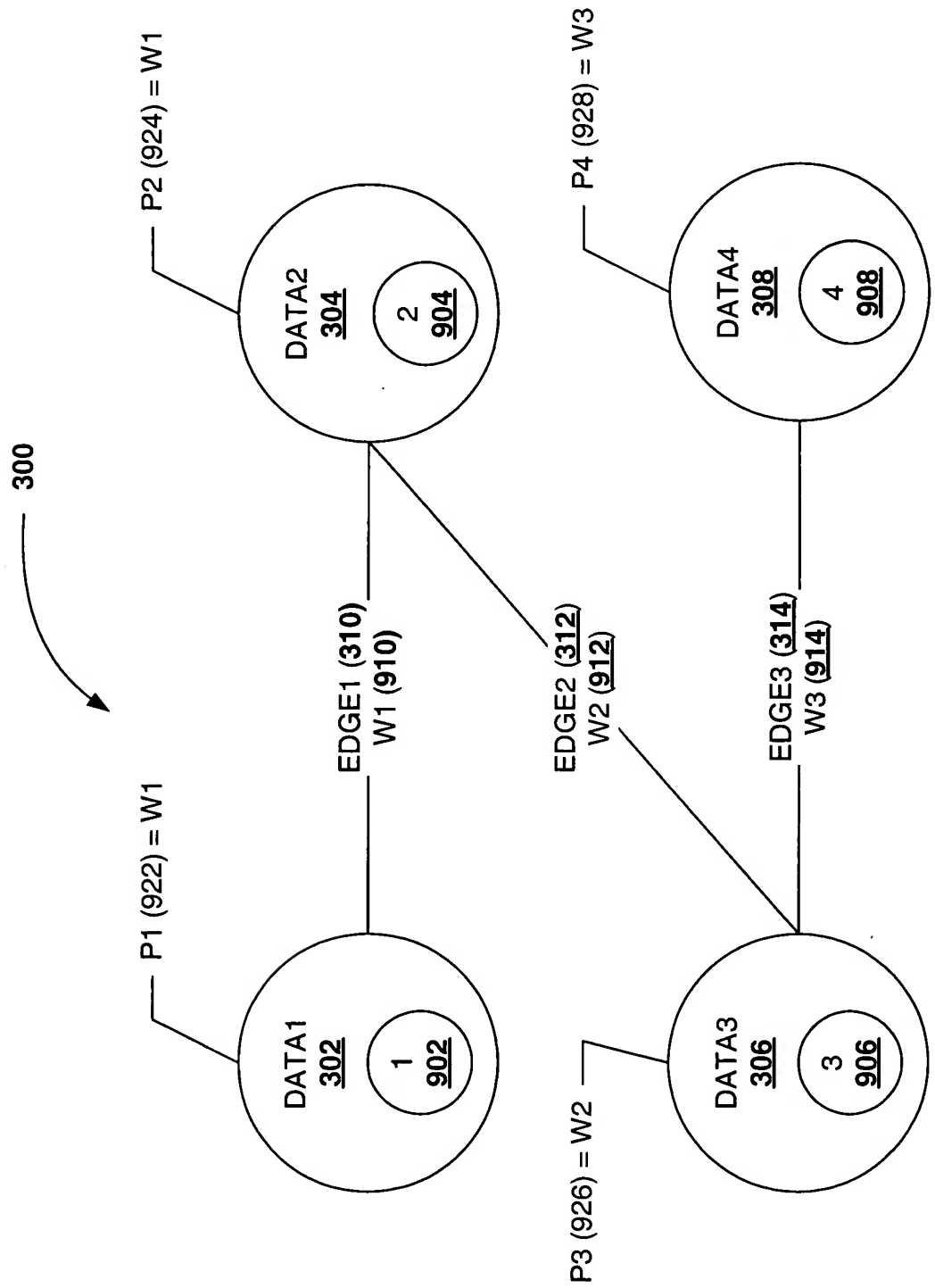
300
P1 (922) = W1
DATA1
302
1
902
P2 (924) = W1
DATA2
304
2
904
P3 (926) = W2
DATA3
306
3
906
P4 (928) = W3
DATA4
308
4
908
EDGE1 (310)
W1 (910)
EDGE2 (312)
W2 (912)
EDGE3 (314)
W3 (914)

FIG. 9

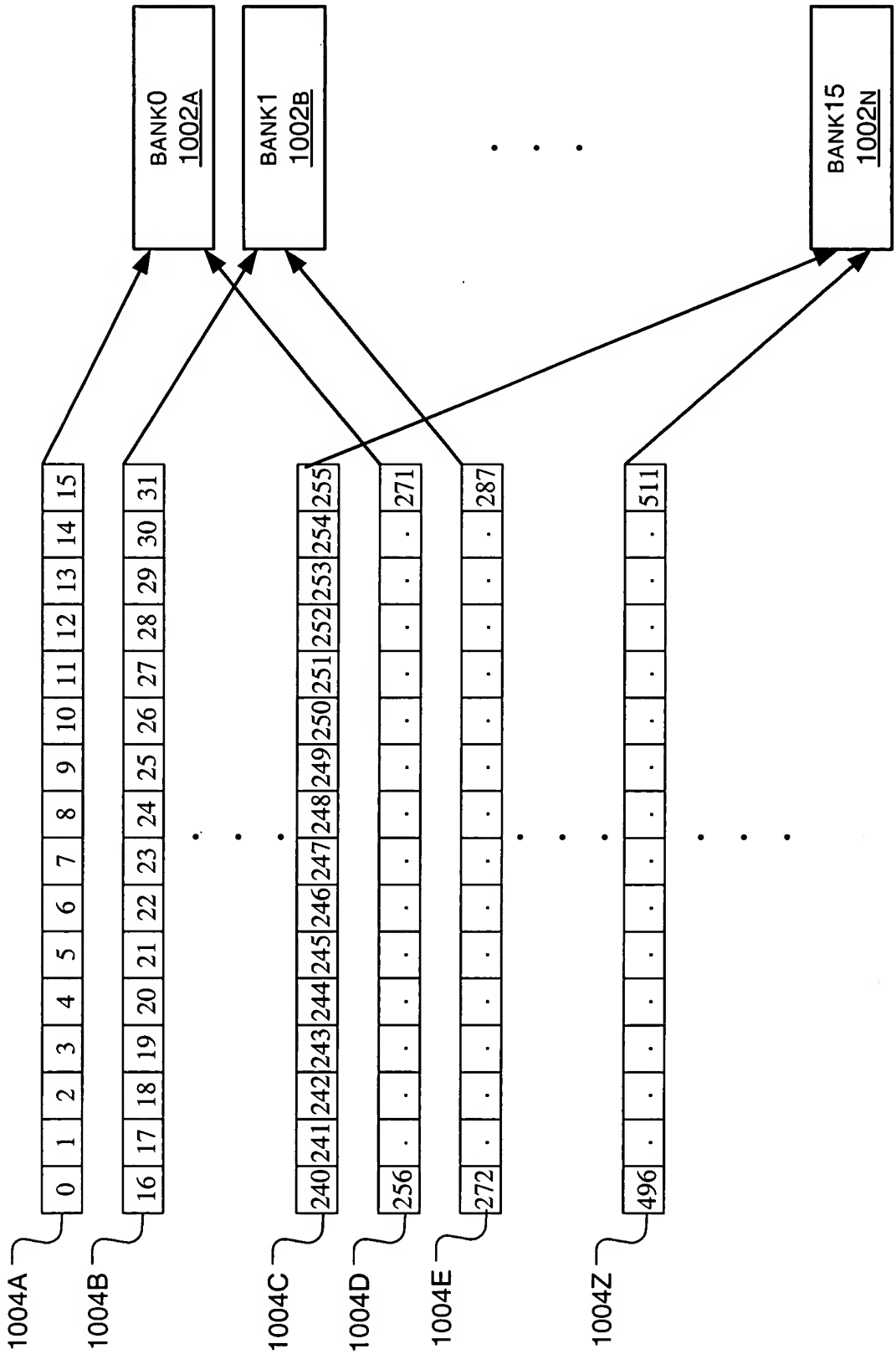
BANK0
1002A
BANK1
1002B
BANK15
1002N
1004A
1004B
1004C
1004D
1004E
1004Z
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255
256 271
272 287
496 511

FIG. 10

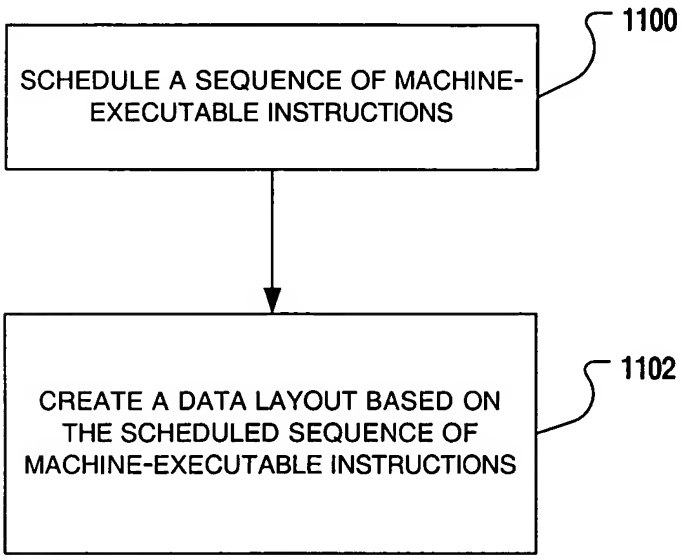
1100
SCHEDULE A SEQUENCE OF MACHINE-EXECUTABLE INSTRUCTIONS
1102
CREATE A DATA LAYOUT BASED ON THE SCHEDULED SEQUENCE OF MACHINE-EXECUTABLE INSTRUCTIONS

FIG. 11

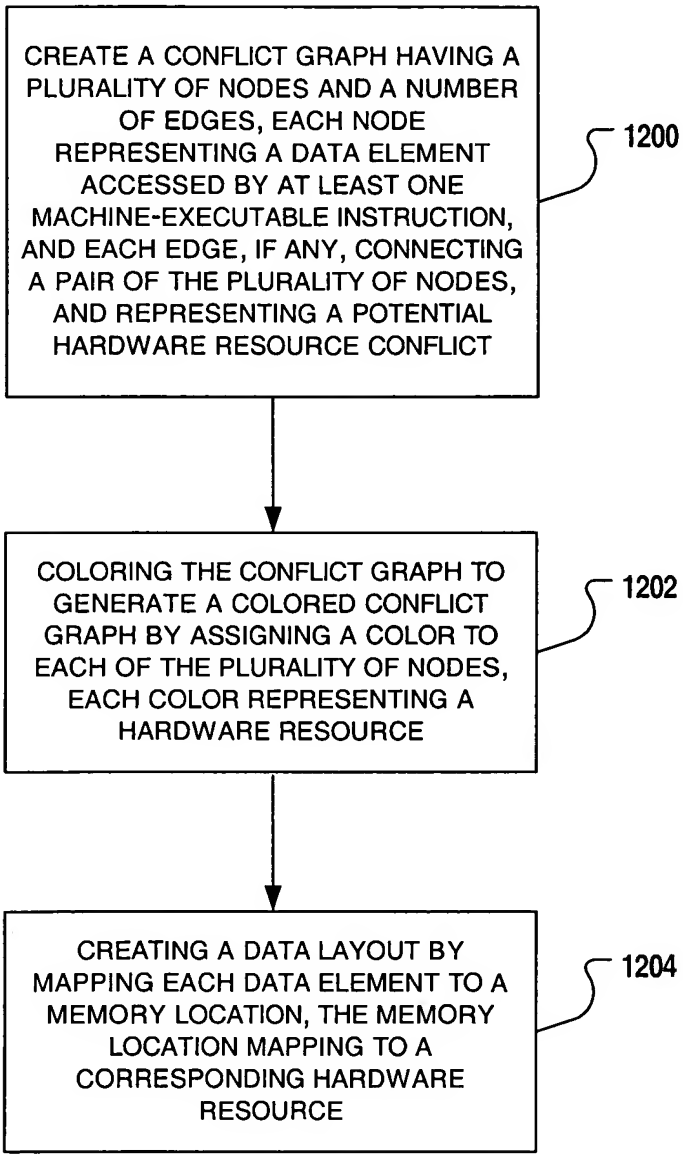
CREATE A CONFLICT GRAPH HAVING A PLURALITY OF NODES AND A NUMBER OF EDGES, EACH NODE REPRESENTING A DATA ELEMENT ACCESSED BY AT LEAST ONE MACHINE-EXECUTABLE INSTRUCTION, AND EACH EDGE, IF ANY, CONNECTING A PAIR OF THE PLURALITY OF NODES, AND REPRESENTING A POTENTIAL HARDWARE RESOURCE CONFLICT
1200
COLORING THE CONFLICT GRAPH TO GENERATE A COLORED CONFLICT GRAPH BY ASSIGNING A COLOR TO EACH OF THE PLURALITY OF NODES, EACH COLOR REPRESENTING A HARDWARE RESOURCE
1202
CREATING A DATA LAYOUT BY MAPPING EACH DATA ELEMENT TO A MEMORY LOCATION, THE MEMORY LOCATION MAPPING TO A CORRESPONDING HARDWARE RESOURCE
1204

FIG. 12